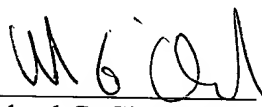


REMARKS

Claims 94-98, 100, 102, 104, and 106 added by this Amendment are copies claims 1, 3-6, 12, 15, 18, and 21, respectively, of U.S. Patent No. 6,381,172 of Banks, granted issued April 30, 2002. Claims 99, 101, 103, and 105 added by this Amendment are substantial copies of the pairs of claims 7 and 8, 13 and 14, 16 and 17, and 19 and 20, respectively, of U.S. Patent No. 6,381,172, differing from the originals in the '172 patent in that they do not specify the phenomenon of hot electron injection for injecting electrons into the floating gate. A copy of U.S. Patent No. 6,381,172 of Banks is being filed herewith for the convenience of the Examiner.

An early examination and allowance of the present application are solicited.

Respectfully submitted,



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## Appendix

### Pending Claims

(Claims 1-62 have been cancelled.)

63. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

64. The method of operating the electrically alterable non-volatile multi-level memory according to claim 63, wherein the operation for settling the parameter includes a

program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

65. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

verifying whether the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state selected from the plurality of states by comparing the electrical value of the one non-volatile multi-level memory cell with a plurality of verifying reference electrical values including at least a first verifying reference electrical value, a second verifying reference electrical value, a third verifying reference electrical value and a fourth verifying reference electrical value, and of repeating the operation for controlling the electrical value and the operation for verifying until it is verified by the operation for verifying that the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state,

reading status of the one non-volatile multi-level memory cell by comparing the electrical value with a plurality of reading reference electrical values including at least a first

reading reference electrical value, a second reading reference electrical value and a third reading reference electrical value,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference electrical value is allocated between the first state and the second state, the second reading reference electrical value is allocated between the second state and the third state, and the third reading reference electrical value is allocated between the third state and the fourth state,

wherein the first reading reference electrical value, the second reading reference electrical value and the third reading reference electrical value are electrical values for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the electrical value with the plurality of reading reference electrical values by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the electrical value from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference electrical value, a second input terminal of the second sense circuit is supplied with the second reading reference electrical value and a second input terminal of the third sense circuit is supplied with the third reading reference electrical value, and

wherein the first verifying reference electrical value is allocated below the first reading reference electrical value, the second verifying reference electrical value is allocated between the first reading reference electrical value and the second reading reference electrical value, the third verifying reference electrical value is allocated between the second reading reference electrical value and the third reading reference electrical value and the fourth verifying reference electrical value is allocated above the third reading reference electrical value.

66. The method of operating the electrically alterable non-volatile multi-level memory according to claim 65, wherein the operation for controlling the electrical value

includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

67. An electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction:

wherein an operation for settling a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state is carried out in response to information to be stored in the one non-volatile multi-level memory cell,

wherein an operation of verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states is carried out by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter is carried out, and repeating the operation for settling the parameter and the operation for verifying are carried out until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

wherein an operation of reading status of the one non-volatile multi-level memory cell is carried out by comparing the parameter with a plurality of reading reference parameters

including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the parameter with the plurality of reading reference parameters by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter, and

wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

68. The electrically alterable non-volatile multi-level memory according to claim 67, wherein the operation for settling the parameter includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

69. The electrically alterable non-volatile multi-level memory according to claim 68, further comprising, a plurality of bit lines, including said first and said second bit line, each of which transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said first group in said matrix are coupled to said first bit line of said plurality of bit lines, drain regions of said multi-level memory cells of said second group adjoining to said first group in said matrix are coupled to said second bit line adjoining to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells of a third group adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines

70. An electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential, electrons being capable of being injected into the floating gate from the channel of each of the plurality of non-volatile multi-level memory cell, electric currents flowing through the channels of the multi-level memory cells of the first group and electric currents flowing through the channels of the multi-level memory cells of the second group being substantially flowing in a same direction:

wherein an operation for controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state is carried out in response to information to be stored in the one non-volatile multi-level memory cell,

wherein an operation for verifying whether the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state selected from the plurality of states is carried out by comparing the electrical value of the one non-volatile multi-level memory cell with a plurality of verifying reference electrical values including at least a first



verifying reference electrical value, a second verifying reference electrical value is carried out, a third verifying reference electrical value and a fourth verifying reference electrical value, and repeating the operation for controlling the electrical value and the operation for verifying are carried out until it is verified by the operation for verifying that the electrical value of the one non-volatile multi-level memory cell has being controlled to the one state,

wherein an operation for reading status of the one non-volatile multi-level memory cell is carried out by comparing the electrical value with a plurality of reading reference electrical values including at least a first reading reference electrical value, a second reading reference electrical value and a third reading reference electrical value,

wherein a conductivity value of the one non-volatile multi-level memory cell is decreased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference electrical value is allocated between the first state and the second state, the second reading reference electrical value is allocated between the second state and the third state, and the third reading reference electrical value is allocated between the third state and the fourth state,

wherein the first reading reference electrical value, the second reading reference electrical value and the third reading reference electrical value are electrical values for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

wherein the normal read operation is carried out by parallel-comparing the electrical value with the plurality of reading reference electrical values by using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the electrical value from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference electrical value, a second input terminal of the second sense circuit is supplied with the second reading reference electrical value and a second input terminal of the third sense circuit is supplied with the third reading reference electrical value, and

wherein the first verifying reference electrical value is allocated below the first reading reference electrical value, the second verifying reference electrical value is allocated between the first reading reference electrical value and the second reading reference electrical value, the third verifying reference electrical value is allocated between the second reading

reference electrical value and the third reading reference electrical value and the fourth verifying reference electrical value is allocated above the third reading reference electrical value.

71. The electrically alterable non-volatile multi-level memory according to claim 70, wherein the operation for controlling the electrical value includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell

72. The electrically alterable non-volatile multi-level memory according to claim 71, further comprising, a plurality of bit lines, including said first and said second bit line, each of which transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said first group in said matrix are coupled to said first bit line of said plurality of bit lines, drain regions of said multi-level memory cells of said second group adjoining to said first group in said matrix are coupled to said second bit line adjoining to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells of a third group adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines.

73. An electrically non-volatile multi-level memory device comprising:  
a plurality of memory cells disposed in matrix having rows and columns,  
wherein each of said plurality of memory cells has a threshold voltage corresponding to data of two bits,

wherein threshold voltages of said plurality of memory cells are allocated to one of a first, a second, a third and a fourth threshold range,

wherein said first threshold range indicates an erase state, and said second, said third, said fourth threshold range indicate program states different from said erase state,

wherein said second, said third and said fourth threshold range indicate mutually different programming states,

wherein a threshold voltage of a memory cell selected from said plurality of memory cells is allocated in one of said first, said second and said third threshold range, and

wherein control gates of memory cells on the same row in said matrix are coupled to a word line of a plurality of word lines,

a plurality of bit lines each of which transfers information indicating data stored in a memory cell, wherein drain regions of memory cells on a first column in said matrix are coupled to a first bit line of said plurality of bit lines, drain regions of memory cells on a second column adjoining to said first column in said matrix are coupled to a second bit line adjoining to said first bit line in said plurality of bit lines and drain regions of memory cells on a third column adjoining to said second column in said matrix are coupled to a third bit line adjoining to said second bit line in said plurality of bit lines,

a programming circuit programming ones of said plurality of memory cells to said programming states by using verify reference parameters,

a sense circuit which compares information indicating data stored in a memory cell with a first reference parameter, a second reference parameter and a third reference parameter in parallel, in a normal read operation,

wherein said first threshold range is lower than said second threshold range, said second threshold range is lower than said third threshold range, and said third threshold range is lower than said fourth threshold range,

wherein said third reference parameter is higher than said second reference parameter, and said second reference parameter is higher than said first reference parameter,

wherein said verify reference parameters have at least first and second verify reference parameters,

wherein said first verify reference parameter is allocated between said second threshold range and said third threshold range, and said second verify reference parameter is allocated between said first threshold range and said second threshold range, and

wherein said first verify reference parameter is settled between said second reference parameter and said third reference parameter, and said second verify reference parameter is settled between said first reference parameter and said second reference parameter

74. An electrically non-volatile multi-level memory device according to claim 73, wherein each of said plurality of memory cells has a floating gate, and a threshold voltage of a selected memory cell is allocated to one of said first, said second and said third threshold

range from said fourth threshold range by being injected with hot electron to a floating gate of said selected memory cell

75. An electrically non-volatile multi-level memory device according to claim 74, further comprising,

a column select circuit which receives column addresses, and which couples selected bit lines to said sense circuits

76. An electrically non-volatile multi-level memory device according to claim 75, wherein each of said sense circuits has a first comparator which receives said information and said first reference parameter, a second comparator which receives said information and said second reference parameter and a third comparator which receives said information and said third reference parameter

77. An electrically non-volatile multi-level memory device according to claim 75, wherein each of said plurality of memory cells has a source region to which is supplied with a reference potential in said read operation.

78. A storage device used for an information processing device comprising:  
a cache memory operably connected to a CPU of said information processing device;  
and

a flash memory operably connected to said cache memory and used as a main memory for said storage device.

79. A storage device used for an information processing device comprising:  
a cache memory operably connected to a microprocessor of said information processing device; and

a flash memory operably connected to said cache memory and used as a primary memory for said storage device.

80. For an electrically alterable non-volatile multi-level semiconductor memory device including a plurality of non-volatile multi-level memory cells, each of the

multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a bit line and a reference potential, electrons being capable of being injected into the floating gate from the channel in each of the plurality of non-volatile multi-level memory cells, a method of operating the electrically alterable non-volatile multi-level semiconductor memory device, comprising:

setting a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

when one of the first third states is selected, verifying whether the parameter of the one non-volatile multi-level memory cell has been set to the one state, including comparing the parameter of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter and a third verifying reference parameter, the operation of setting the parameter being conducted until it is verified by the operation of verifying that the parameter of the one non-volatile multi-level memory cell has been set to the one state,

reading status of the one non-volatile multi-level memory cell, including comparing the parameter of the one non-volatile multi-level memory cell, with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read

operation in which the information stored in the one non-volatile multi-level memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter of the one non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter,

wherein the first verifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter, and

wherein the plurality of non-volatile multi-level memory cells of the matrix of the rows and the columns are disposed in substantially a rectangle that has a first side, a second side, a third side and a fourth side, the first side and the second side intersect with each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multi-level memory cells and the first side of the rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and latches, is disposed at the second side of the rectangle.

81. The method of operating the electrically alterable non-volatile multi-level memory according to claim 80,

wherein the operation of setting the parameter includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

82. The method of operating the electrically alterable non-volatile multi-level memory according to claim 81,

wherein the operation of setting the parameter includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

83. For an electrically alterable non-volatile multi-level semiconductor memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a bit line and a reference potential, electrons being capable of being injected into the floating gate from the channel in each of the plurality of non-volatile multi-level memory cells, a method of operating the electrically alterable non-volatile multi-level semiconductor memory device, comprising:

controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell,

when one of the first to third states is selected, verifying whether the electrical value of the one non-volatile multi-level memory cell has been controlled to the one state, including comparing the electrical value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference electrical values including at least a first verifying reference electrical value, a second verifying reference electrical value and a third verifying reference electrical value, the operation of controlling the electrical value being conducted until it is verified by the operation of verifying that the electrical value of the one non-volatile multi-level memory cell has been controlled to the one state,

reading status of the one non-volatile multi-level memory cell, including comparing the electrical value of the one non-volatile multi-level memory cell with a plurality of reading reference electrical values including at least a first reading reference electrical value, a second reading reference electrical value and a third reading reference electrical value,

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference electrical value is allocated between the first state and the second state, the second reading reference electrical value is allocated between the second state and the third state, and the third reading reference electrical value is allocated between the third state and the fourth state,

wherein the first reading reference electrical value, the second reading reference electrical value and the third reading reference electrical value are electrical values for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the electrical value of the one non-volatile multi-level memory cell with the plurality of reading reference electrical values using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the electrical value from the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference electrical value, a second input terminal of the second sense circuit is supplied with the second reading reference electrical value and a second input terminal of the third sense circuit is supplied with the third reading reference electrical value,

wherein the first verifying reference electrical value is allocated above the first reading reference electrical value, the second verifying reference electrical value is allocated between the first reading reference electrical value and the second reading reference electrical value and the third verifying reference electrical value is allocated between the second reading reference electrical value and the third reading reference electrical value, and

wherein the plurality of non-volatile multi-level memory cells of the matrix of the rows and the columns are disposed in substantially a rectangle that has a first side, a



second side, a third side and a fourth side, the first side and the second side intersect with each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multi-level memory cells and the first side of the rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and latches, is disposed at the second side of the rectangle.

84. The method of operating the electrically alterable non-volatile multi-level memory according to claim 83,

wherein the operation of controlling the electrical value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

85. The method of operating the electrically alterable non-volatile multi-level memory according to claim 84,

wherein the operation of controlling the electrical value includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

86. An electrically alterable non-volatile multi-level semiconductor memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a bit line and a reference potential, electrons being capable of being injected into the floating gate from the channel in each of the plurality of non-volatile multi-level memory cells,

wherein an operation of setting a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to a state selected

from a plurality of states including at least a first state, a second state, a third state and a fourth state is carried out in response to information to be stored in the one non-volatile multi-level memory cell,

wherein, when one of the first to third states is selected, an operation of verifying whether the parameter of the one non-volatile multi-level memory cell has been set to the one state is carried out and includes comparing the parameter of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter and a third verifying reference parameter, and the operation of setting the parameter is conducted until it is verified by the operation of verifying that the parameter of the one non-volatile multi-level memory cell has been set to the one state,

wherein an operation of reading status of the one non-volatile multi-level memory cell is carried out and includes comparing the parameter of the one non-volatile multi-level memory cell with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter of the none non-volatile multi-level memory cell with the plurality of reading reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is

supplied with the first reading reference parameter, a second input terminal of the second sense circuit is supplied with the second reading reference parameter and a second input terminal of the third sense circuit is supplied with the third reading reference parameter,

wherein the first verifying reference parameter is allocated above the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter and the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter, and

wherein the plurality of non-volatile multi-level memory cells of the matrix of the rows and the columns are disposed in substantially a rectangle that has a first side, a second side, a third side and a fourth side, the first side and the second side intersect with each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multi-level memory cells and the first side of the rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and latches, is disposed at the second side of the rectangle.

87. The electrically alterable non-volatile multi-level memory according to claim 86,

wherein the operation of setting the parameter includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

88. The electrically alterable non-volatile multi-level memory according to claim 87,

wherein each of the operation of setting the parameter includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

89. The electrically alterable non-volatile multi-level memory according to claim 88,

wherein each of the plurality of bit lines transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said group in said matrix are coupled to a first bit line of said plurality of bit lines, drain regions of multi-level memory cells of a second group adjacent to said group in said matrix are coupled to a second bit line adjacent to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells of a third group adjacent to said second group in said matrix are coupled to a third bit line adjacent to said second bit line in said plurality of bit lines.

90. An electrically alterable non-volatile multi-level semiconductor memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, the plurality of non-volatile multi-level memory cells being disposed in a matrix of rows and columns, channels of multi-level memory cells of a group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a bit line and a reference potential, electrons being capable of being injected into the floating gate from the channel in each of the plurality of non-volatile multi-level memory cells,

wherein an operation of controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to a state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state is carried out in response to information to be stored in the one non-volatile multi-level memory cell,

wherein, when one of the first to third states is selected, an operation of verifying whether the electrical value of the one non-volatile multi-level memory cell has been controlled to the one state is carried out and includes comparing the electrical value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference electrical values including at least a first verifying reference electrical value, a second verifying reference electrical value and a third verifying reference electrical value, and the operation of controlling the electrical value is conducted until it is verified by the operation of verifying that the electrical value of the one non-volatile multi-level memory cell has been controlled to the one state,

wherein an operation of reading status of the one non-volatile multi-level memory cell is carried out and includes comparing the electrical value of the one non-volatile multi-level memory cell with a plurality of reading reference electrical values including at least a first reading reference electrical value, a second reading reference electrical value and a third reading reference electrical value,

wherein a conductivity value of the one non-volatile multi-level memory cell is increased in order of the first state, the second state, the third state and the fourth state,

wherein the first reading reference electrical value is allocated between the first state and the second state, the second reading reference electrical value is allocated between the second state and the third state, and the third reading reference electrical value is allocated between the third state and the fourth state,

wherein the first reading reference electrical value, the second reading reference electrical value and the third reading reference electrical value are electrical values for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the electrical value of the one non-volatile multi-level memory cell with the plurality of reading reference electrical values using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the electrical value of the one non-volatile multi-level memory cell, a second input terminal of the first sense circuit is supplied with the first reading reference electrical value, a second input terminal of the second sense circuit is supplied with the second reading reference electrical value and a second input terminal of the third sense circuit is supplied with the third reading reference electrical value,

wherein the first verifying reference electrical value is allocated above the first reading reference electrical value, the second verifying reference electrical value is allocated between the first reading reference electrical value and the second reading reference electrical value and the third verifying reference electrical value is allocated between the second reading reference electrical value and the third reading reference electrical value, and

wherein the plurality of non-volatile multi-level memory cells of the matrix of the rows and the columns are disposed in substantially a rectangle that has a first side, a

second side, a third side and a fourth side, the first side and the second side intersect with each other substantially perpendicularly, a plurality of word lines coupled with gate electrodes of floating gate FET's of the multi-level memory cells and the first side of the rectangle intersect with each other substantially perpendicularly, a plurality of bit lines coupled with drains of floating gate FET's of the multi-level memory cells and the second side of the rectangle intersect with each other substantially perpendicularly, a row select circuit is disposed at the first side of the rectangle for coupling with the plurality of word lines, and peripheral circuitry, including a column select circuit, sense circuits, a data conversion circuit and latches, is disposed at the second side of the rectangle.

91. The electrically alterable non-volatile multi-level memory according to claim 90,

wherein the operation of controlling the electrical value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

92. The electrically alterable non-volatile multi-level memory according to claim 91,

wherein the operation of controlling the electrical value includes a program operation in which electrons are injected into a floating gate of the one non-volatile multi-level memory cell.

93. The electrically alterable non-volatile multi-level memory according to claim 92,

wherein each of the plurality of bit lines transfers information indicating data stored in a memory cell, wherein drain regions of said multi-level memory cells of said group in said matrix are coupled to a first bit line of said plurality of bit lines, drain regions of said multi-level memory cells of a second group adjacent to said group in said matrix are coupled to a second bit line adjacent to said first bit line in said plurality of bit lines and drain regions of multi-level memory cells of a third group adjacent to said second group in said matrix are coupled to a third bit line adjacent to said second bit line in said plurality of bit lines.

94.(New) A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a threshold voltage representing data of at least two bits, wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state;

parameter generating circuitry generating a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter; and

sensing/program-verifying circuitry receiving a parameter which represents threshold voltage of one non-volatile memory cell, the first programming reference parameter, the first read reference parameter, the second programming reference parameter, the second read reference parameter, the third programming reference parameter and the third read reference parameter;

wherein the first read reference parameter is allocated between a level corresponding to the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold

level indicating the erase state, and one of the first programming reference parameter and the first read reference parameter is shifted from and dependent upon the other,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level, and one of the second programming reference parameter and the second read reference parameter is shifted from and dependent upon the other, and

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level, and one of the third programming reference parameter and the third read reference parameter is shifted from and dependent upon the other.

95.(New) A non-volatile semiconductor memory device according to claim 94,

wherein the parameter generating circuitry includes a first parameter generating circuit which generates the first programming reference parameter and the first read reference parameter, a second parameter generating circuit which generates the second programming reference parameter and the second read reference parameter, and a third parameter generating circuit which generates the third programming reference parameter and the third read reference parameter, and

wherein each of the first parameter generating circuit, the second parameter generating circuit and the third parameter generating circuit includes an element causing the corresponding one reference parameter and the corresponding other reference parameter to have different values.

96.(New) A non-volatile semiconductor memory device according to claim 95,

wherein each of the first parameter generating circuit, the second parameter generating circuit and the third parameter generating circuit further includes a reference cell



which has substantially the same construction as each of said plurality of memory cells, and the reference cell and the element of each parameter generating circuit cooperate to provide a predetermined difference between the corresponding read and programming reference parameters.

97.(New) A non-volatile semiconductor memory device according to claim 94,

wherein each read reference parameter is dependent upon the corresponding programming reference parameter.

98.(New) A non-volatile semiconductor memory device according to claim 94,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

99.(New) A non-volatile semiconductor memory device according to claim 98,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

100.(New) A non-volatile semiconductor memory device according to claim 95,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

101.(New) A non-volatile semiconductor memory device according to claim 12,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by hot electron injection.

102.(New) A non-volatile semiconductor memory device according to claim 96,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

103.(New) A non-volatile semiconductor memory device according to claim 102,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

104.(New) A non-volatile semiconductor memory device according to claim 5,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the threshold level indicating the erase state, the first threshold level, the second threshold level and the third threshold level, and

wherein threshold voltages of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the threshold level indicating the erase state by an erase operation.

105.(New) A non-volatile semiconductor memory device according to claim 104,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel.

106.(New) A non-volatile semiconductor memory device according to claim 94,

wherein the first, second and third read reference parameters are dependent upon the first, second and third programming reference parameters, respectively.